sbRIO Digital Communication Within the Multi-sensor Excitation Low Voltage Chassis

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This note discusses the communication signals to and from the single-board Compact RIO (sbRIO), analog-to-digital converters (ADCs), and digital-to-analog converters (DACs) inside the Multi-sensor Excitation Low Voltage (MSELV) chassis.

For Hall B magnets' MSELV chassis upgrade [1], two LabVIEW subVIs were developed—one for communication between the sbRIO FPGA and the MSELV's ADCs and the other for communication between the sbRIO FPGA and MSELV's DACs. The sbRIO FPGA uses digital serial communication to shift data in binary format to and from ADCs and to DACs.

For the ADCs and DACs, the sbRIO generates a 3.3 V digital signal for the serial clock (SCLK), data input (DIN), and the signal which indicates to the ADCs and DACs to prepare for communication–chip select (CS) for the ADCs, synchronize (SYNC) for the DACs. There is an additional signal for the ADC–data output (DOUT).

Sensor data readout rate of the present MSELV chassis is 1 Hz; hence slower communication settings are used in the sbRIO FPGA subVIs, Table I.

An example of the sbRIO's communication to the ADC and the ADC's response is shown in Fig.1. CS is used to signal the ADC to prepare for data input. On the first rising clock edge after CS toggles low, the sbRIO begins writing the eight-bit 00110000 DIN signal to the ADC. During this period, any signal observed on the DOUT line is ignored.

The DIN signal initiates the ADC to respond with the data for the channel that the ADC has most recently read. After the eighth DIN bit, the ADC responds with a 32-bit DOUT signal. During this time, any signal received by the ADC on the DIN line is ignored.

The first three bits of DOUT (100b in Fig. 1) indicate status. The first bit indicates whether the data communicated is new, the second whether the channel's input is over the ADC's input range, and the third whether the ADC's power supply is inadequate. For these bits, a 0 indicates that the status is false, 1 that it is true.

The next five bits of DOUT (01000b in Fig. 1) are the ADC channel's register address. Table II shows the register addresses for the 16 single-ended, ADC input channels.

ADC counts measured for the channel specified by the address bits is given by the last 24 bits of DOUT, this binary sequence is converted to a decimal and then to a voltage.

Device	Property	Min. timing possible [ns]	Used in sbRIO [ns]
DAC	SCLK period	20	20,000
	SCLK high/low time	8	10,000
	data setup time	6	6,000
	data hold time	4	4,000
ADC	SCLK period	~120	4,000
	SCLK high/low time	~50	2,000
	data setup time	10	1,000
	data hold time	5	1,000
	propagation delay at start of DOUT	20	N/A

TABLE I. ADC and DAC timing specifications; minimum timing possible for ADCs and DACs and the settings used.

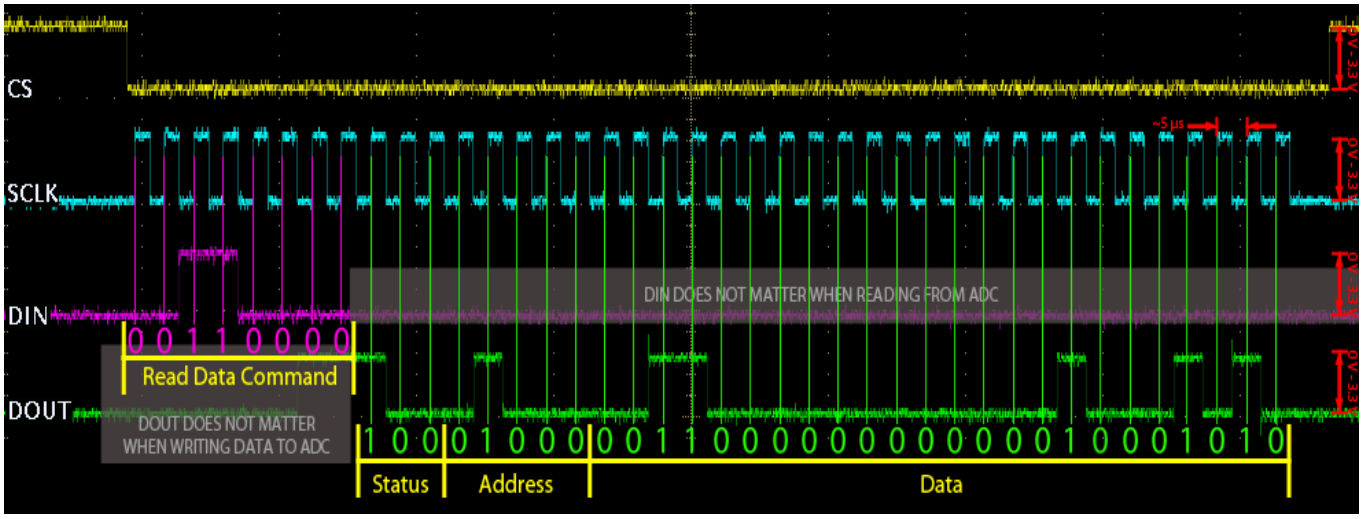

FIG. 1. ADC communication signals between sbRIO and an ADC channel.

ADC channel	Register address
0	01000b
1	01001b
2	01010b
3	01011b
4	01100b
5	01101b
6	01110b
7	01111b
8	10000b
9	10001b
10	10010b
11	10011b
12	10100b
13	10101b
14	10110b
15	10111b

TABLE II. Register address bits of the single-ended ADC channels .

An example of sbRIO's communication with the DAC is shown in Fig. 2. The SYNC signal is used to ready the DAC to receive commands. Data is written to the DAC as a 32-bit DIN signal. Bits 0–3 (0000b in Fig. 2) are the prefix bits. The first prefix bit must be zero for data to be written to the DAC; the remaining three prefix bits are irrelevant.

Bits 4–7 are control bits that indicate what the DAC should do. For the MSELV chassis, the control bits are always 0011b for setting the DAC and enabling the channel designated by the address bits 8–11. Table III contains the DAC channels and their corresponding address bits.

DAC channel	Address bits
A	0000b
B	0001b
C	0010b
D	0011b
E	0100b
F	0101b
G	0110b
H	0111b

TABLE III. DAC channels and their respective address bits.

Bits 12–27 are the DAC counts that correspond to voltage to output on the DAC channel. DAC counts are converted from voltage.

The final four bits 28–31, feature bits, enable certain features of the DAC. For the MSELV chassis, all four feature bits are 0000b.

In summary, the developed sbRIO subVIs have been able to successfully communicate with the DACs and ADCs in the MSELV chassis. These subVIs make up the basic drivers for communication between the MSELV chassis and sbRIO and enable the sbRIO to take the place of the previously used DE0-Nano FPGA.

[1] T. Lemon, et al. *sbRIO-based Multi-Sensor Excitation Low Voltage Chassis for Hall B Magnets*, DSG Note 2019-43, 2019.

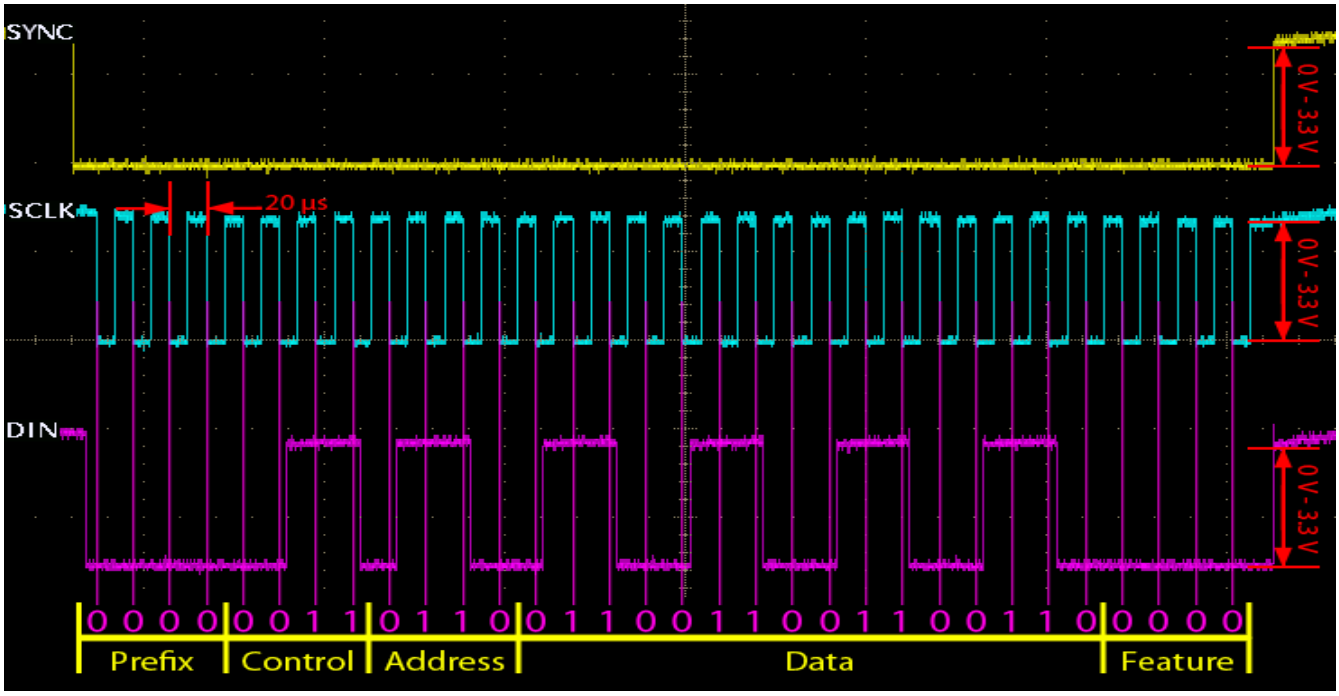

FIG. 2. DAC communication signals.